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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/986,299	11/08/2001	Takashi Hiroi	501.40830X00	5170

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EXAMINER	
STREGE, JOHN B	
ART UNIT	PAPER NUMBER
2625	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,299	HIROI ET AL.	
	Examiner	Art Unit	
	John B Strege	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *1-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner's Comment

The substitute specification has been received and entered. Claims 1-15 are pending and claims 16-27 have been cancelled.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-15 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 16-27 of copending Application No. 09986577. Claims 1-15 are directed to a method for pattern inspection and claims 16-27 are directed to an apparatus. Method and apparatus claims are not patentably distinct. Furthermore, although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations are only worded differently however have similar subject matter.

Claim 1 of the instant application discloses, "A pattern inspection method comprising the steps of: attaining a digital image of an object substrate through

microscopic observation thereof (claim 17 of the copending application lines 1-3); detecting defects in examination of the attained digital image while masking a pre-registered region or a pattern meeting a pre-registered pattern (claim 17 of the copending application lines 4-6); and outputting an image of each of the defects thus detected together with position-on-substrate data thereof (claim 17 of the copending application lines 8-9).

Furthermore the additional limitations that exist in some of the claims such as a memory part for storing coordinated data of a non-inspection region to be masked (claim 16) are well known in the art as disclosed by Murase USPN 5,321,767 (further cited in the 103 rejection below). Murase discloses determining the position of examination region or mask in step 17 of figure 2.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

3. Claims 1-15 are objected to because of the following informalities: Each of the claims contains examples of single words separated by spaces such as "objec t" in line 2 of claim 1. Appropriate correction for all of these occurrences in the claims is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inokuchi USPN 6,259,960 in view of Murase USPN 5,321,767.

Inokuchi discloses a part-inspecting system for detecting the presence of a defect on an inspected part, such as a silicon wafer, storing information about defects, and using the stored information for later operations to detect defects on parts (col. 1 lines 4-14). When a part to be inspected, i.e., a wafer on which a pattern is formed, is placed in position for inspection the optical defect-inspecting apparatus 02 (figure 72) automatically detects the size and position of any defect (col. 2 lines 16-22). This forms the preliminary inspection step and an optical microscope can be used (col. 3 lines 35-36 and lines 43-46). The preliminary inspection information files can be displayed as shown in figures 73A and 73 B (col. 2 lines 41-56) where 73A shows the contour of a wafer under inspection, as well as the positions of defects on the inspected part and 73B shows the defect position, sizes, and other information. The operator watches the images of figures 73A and 73B and manually specifies the defect that he wants to review closer using a scanning electron microscope (col.3 lines 20-30).

Inokuchi does not explicitly disclose detecting defects of the attained digital image while masking a pre-registered region or pattern.

Murase discloses a method forming a mask in an image processing operation for indicating a non-examination region that is to be excluded from the inspection of the

appearance of articles (col. 1 lines 8-12, and col. 3 lines 57-60). As seen in figure 6, one possible article of inspection is an integrated circuit 26 (col. 5 lines 46-47). Murase recites that there is a problem in the prior art with inspecting articles when non-critical spots on the article such as printed letters show up as defects, and it is difficult to discriminate between defective parts and the letters (col. 2 line 61 – col. 3 line 10). Murase further recites that such a problem would be overcome by forming a masking region that would conceal the printed letters so as to neglect the data carried by the pixels inside such a mask (col. 3 lines 10-14).

Inokuchi and Murase are analogous art because they are from the same field of endeavor of inspection of semiconductor materials.

At the time of the invention it would have been obvious to one of ordinary skill in the art to combine Inokuchi and Murase to obtain a microscopic inspection device that takes an image of a semiconductor and masks out defects that are non-critical. The motivation for doing so is that it would speed up the process of inspection by not having to take into account uncritical areas. Thus, it would have been obvious to one of ordinary skill in the art to combine Inokuchi and Murase to obtain the invention as specified in claim 1.

Regarding claim 2, Murase discloses that taking an image of the object to obtain image data and processing said image data by an image processing apparatus where a mask indicating a non-examination region which is to be set is decided from the image (col. 3 lines 52-60). As discussed Inokuchi discloses the microscopic observation step.

Regarding claim 3, as seen in figure 73a of Inokuchi, data regarding the entire wafer is output in the preliminary step. As discussed Inokuchi discloses that the operator watches the images of figures 73a and 73b and lists the defects that might adversely affect the quality of the inspected part and specifies the defects that he or she wants to review (col. 3 lines 20-25), thus all defects critical and non-critical are seen by the operator. Combining this with Murase, it would be obvious to output the defects found on the entire wafer including the masked regions so that an operator reviewing the wafer would know which defects have been masked as non-critical and which defects are critical, thus avoiding confusion in later reviews of the wafer.

Claim 4 has similar limitations to claim 3, in that at the data displaying step defects having a feature that meets a pre-registered feature re so indicated as to be distinguishable from the other detected defects. Thus the same arguments used for claim 3 apply equally to claim 4.

Regarding claim 5, this limitation is the same as the limitation of claim 2 already discussed, thus the same arguments used for the rejection of claim 2 apply equally to claim 5.

Regarding claim 6, as seen in figure 73a of Inokuchi, each of the detected defects is displayed on the display screen.

Claims 7-9 are similar to claims 4-6 except that they have the broader interpretation of outputting data instead of displaying the data. In order to display the data it is necessary to output it, thus the arguments used for claims 4-6 apply equally to claims 7-9.

Regarding claim 10, figure 73b of Inokuchi discloses the position and size of the defects as seen on a display viewed by the operator.

Claim 11 is similar to claims 1,4, and 7, with the additional limitations of extracting defects located in predefined regions, classifying the extracted defects through examination, and outputting the class data. Inokuchi discloses that the defect information (figure 22a) about the wafer is searched for defect points having sizes lying in a specified range. Among them, some points Wa and Wb (figure 22b) spaced from each other are extracted (col. 37 lines 43-51). Inokuchi further discloses classifying the defects (at least col. 46 lines 48-56). Furthermore the classified results can be displayed (col. 75 lines 40-44). The rest of the limitations have already been addressed in the previous claims 1, 4, and 7.

Regarding claim 12, as discussed the classified defect is displayed on the screen with the image.

Regarding claim 13, as discussed Inokuchi discloses extracting defects and a reviewer checks the defects based on a preliminary image.

Regarding claims 14-15, it is well known in the art of semiconductor inspection to use CAD, therefore the examiner declares Official Notice. It would have been obvious to one of ordinary skill in the art to use CAD to display the defects since it is a widely used proven method of semiconductor inspection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hennessey et al. USPN 6,246,787 System and method for knowledgebase generation and management.

Levy et al. USPN 4,247,203 Automatic photomask inspection system and apparatus. Especially the definition of mask parameters (col. 15 lines 39-61).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B Strege whose telephone number is (703) 305-8679. The examiner can normally be reached on Monday-Friday between the hours of 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on (703) 308-5246. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JS

YON J. COUSO
PRIMARY EXAMINER